CLAIMS

What is claimed is:

1. A device, comprising:

a memory array in which a plurality of codewords is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data; and

an error code correction module coupled to the memory array;

wherein when multiple units of data are to be read from the device for an address, a codeword stored in a location associated with the address is fetched from the memory array, the error code correction module decodes the codeword and corrects any errors in the data block for that codeword, and the multiple units of data are read from the corrected data block.

2. The device of claim 1, wherein when a single unit of data is to be read from the device for the address, the codeword stored in a location associated with the address is fetched from the memory array, the error code correction module decodes the codeword and corrects any errors in the data block for that codeword, and the single unit of data to be read for the address is read from the corrected data block.

3. The device of claim 1, further comprising a buffer coupled to the memory array, wherein the corrected data block is stored in the buffer and the multiple units of data are read from the buffer.

4. The device of claim 3, wherein the buffer comprises a read buffer.

5. The device of claim 3, wherein the buffer comprises a write buffer.

6. The device of claim 1, further comprising a mode input that indicates how many units of data are to be read from the device for the address.

7. The device of claim 6, wherein the mode input comprises a read/write bit that indicates whether one or more units of data are to be read from or written to the device for the address.

8. A device, comprising:

a memory array in which a plurality of codewords is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data; and

an error code correction module coupled to the memory array;

wherein when multiple units of data are to be written to the device for an address, the multiple units of data are encoded together to generate a codeword and the generated codeword is written to the memory array in a location associated with the address.

9. The device of claim 8, wherein the multiple units of data to be written to the device for the address includes a first number of units of data to be written and each codeword includes a second number of units of data; and

wherein when the multiple units of data are to be written to the device for the address and the first number is less than the second number, a codeword associated with the address is fetched from the memory array, the error code correction module decodes the codeword and corrects any errors in the data block for that codeword, the multiple units of data are inserted into the corrected data block, the corrected data block is encoded to generate the generated codeword, and the generated codeword is written to the memory array in a location associated with the address.

10. The device of claim 8, wherein when a single unit of data is to be written to the device for the address, a codeword associated with the address is fetched from the

memory array, the error code correction module decodes the codeword and corrects any errors in the data block for that codeword, the single unit is inserted into the corrected data block, the corrected data block is encoded to generate the generated codeword, and the generated codeword is written to the memory array in a location associated with the address.

11. The device of claim 8, wherein the multiple units of data are written to the memory array at consecutive addresses starting with the address.

12. The device of claim 8, wherein the memory array includes a magnetic random access memory.

13. The device of claim 8, further comprising a controller that controls the operation of the device.

14. The device of claim 8, wherein the device further includes an address sparing circuit that maps a logical address to a physical address in the memory array.

15. The device of claim 8, wherein each unit of data is equal in size to one or more symbols used by the error code correction module.

16. A method of reading one or more units of data from a memory array in which a plurality of codewords is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data, the method comprising:

when multiple units of data are to be read from the memory array for an address:

fetching the codeword stored in a location associated with the address from the memory array;

decoding the codeword and correcting any errors in the data block for that codeword; and

reading the multiple units of data from the corrected data block.

17. The method of claim 16, further comprising:

when a single unit of data is to be read from the memory array for the address:

fetching the codeword stored in the location associated with the address from the memory array;

decoding the codeword and correcting any errors in the data block for that codeword;

reading the single unit of data to be read for the address from the corrected data block.

18. The method of claim 16, further comprising determining if a read operation or a write operation is to be performed for the address.

19. The method of claim 18, further comprising:

when multiple units of data are to be written to the memory array for the address:

encoding the multiple units of data together to generate a codeword; and

writing the generated codeword in the memory array in the location associated with the address.

20. The method of claim 19, wherein the multiple units of data to be written to the memory array for the address includes a first number of units of data to be written and each codeword includes a second number of units of data; and

further comprising, when the multiple units of data are to be written to the memory array for the address and the first number is less than the second number:

fetching the codeword stored in the location associated with the address from the memory array;

decoding the codeword and correcting any errors in the data block for that codeword;

inserting the multiple units of data into the corrected data block;

encoding the corrected data block to generate the generated codeword; and

writing the generated codeword to the memory array in a location associated with the address.

21. The method of claim 19, further comprising:

when a single unit of data is to be written to the memory array for the address:

fetching the codeword stored in the location associated with the address from the memory array;

decoding the codeword and correcting any errors in the data block for that codeword;

inserting the single unit of data into the corrected data block;

encoding the corrected data block to generate the generated codeword; and

writing the generated codeword to the memory array in a location associated with the address.

22. A method of writing one or more units of data to a memory array in which a plurality of codewords is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data, the method comprising:

when multiple units of data are to be written to the memory array for an address:

encoding the multiple units of data together to generate a codeword; and

writing the generated codeword to the memory array in the location associated with the address.

23. The method of claim 22, wherein the multiple units of data to be written to the memory array for the address includes a first number of units of data to be written and each codeword includes a second number of units of data; and

further comprising, when the multiple units of data are to written to the memory array and the first number is less than the second number:

fetching the codeword stored in the location associated with the address from the memory array;

decoding the codeword and correcting any errors in the data block for that codeword;

inserting the multiple units of data into the corrected data block;

encoding the corrected data block to generate the generated codeword; and

writing the generated codeword to the memory array in the location associated with the address.

24. The method of claim 22, further comprising:

when a single unit of data is to be written to the memory array for the address:

fetching the codeword stored in the location associated with the address from the memory array;

decoding the codeword and correcting any errors in the data block for that codeword;

inserting the single unit of data into the corrected data block;

encoding the corrected data block to generate the generated codeword; and

writing the generated codeword to the memory array in the location associated with the address.

25. A system, comprising:

an assisted memory in which a plurality of codewords is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data; and

a second device coupled to the assisted memory;

wherein when the second device attempts to read multiple units of data from the assisted memory for an address, a codeword stored in a location associated with the address is fetched from the assisted memory, the codeword is decoded, any errors in the data block are corrected for that codeword, and the multiple units of data are read from the corrected data block and supplied to the second device.

26. The system of claim 25, further comprising an interface that couples the assisted memory to the second device.

27. The system of claim 26, wherein the interface comprises a data bus.

28. The system of claim 26, wherein the interface comprises an address bus.

29. The system of claim 26, wherein the interface comprises a clock input.

30. The system of claim 26, wherein the second device comprises a processor.

31. A system, comprising:

an assisted memory in which a plurality of codewords is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data; and

a second device coupled to the assisted memory;

wherein when the second device attempts to write multiple units of data to the assisted memory for an address, the multiple units of data are encoded together to generate a codeword and the generated codeword is written to the assisted memory in a location associated with the address.

32. A device, comprising:

a means for receiving an address;

a means for fetching a codeword stored at a location associated with the address, wherein the codeword comprises a parity block and a data block that comprises a plurality of units of data;

a means for decoding the codeword and correcting any errors in the data block for that codeword; and

a means for reading multiple units of data from the corrected data block.

33. A device, comprising:

a means for receiving an address;

a means for receiving multiple units of data for the address;

a means for encoding the multiple units of data together to generate a codeword, wherein the codeword comprises a data block comprising a plurality of units of data and a parity block generated from the data block; and

a means for storing the generated codeword at a location associated with the address.